AppL No. 10/039,953
Amdt. Dated 1/12/2005
Response to Office action dated 12/21/2004

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Previously presented): A caching system, comprising:

a tail FIFO having a tail input to receive incoming frames containing varying amounts of data and a tail output to output the incoming frames

a memory having a memory input and a memory output, the memory input is coupled to the tail output and the memory is operable to store data from the tail output, and wherein the memory is operable to output the stored data at the memory output;

a multiplexer having first and second multiplexer inputs coupled to the tail output and the memory output, respectively, the multiplexer having a control input to select one of the multiplexer inputs to couple to a multiplexer output;

a head FIFO having a head input coupled to the multiplexer output to receive data from the multiplexer output, and a head output to output frames of the received data; and

a controller coupled to the tail FIFO, the head FIFO, and the memory and operable to transfer a dynamically selected number of blocks of data from the incoming frames having a dynamically selected block size from the tail FIFO to the memory and from the memory to the head FIFO, wherein the selected block size and the selected number of blocks together provide maximum memory transfer efficiency level.

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Claim 2 (Original): The system of claim 1, wherein the head FIFO further comprises a head fill indicator coupled to the controller to indicate a fill characteristic of the head FIFO.

Claim 3 (Previously amended): The system of claim 2, wherein the controller transfers the selected number of blocks of data having the selected block size from the tail FIFO to the memory based on the head fill indicator.

Claim 4 (Currently amended): The system of claim 2, wherein the controller transfers the selected number of blocks of data having the selected block size from the memory to the head FIFO based on the head fill indicator.

Claim 5 (Original): The system of claim 1, wherein the tail FIFO further comprises a tail fill indicator coupled to the controller to indicate a fill characteristic of the tail FIFO.

Claim 6 (Previously amended): The system of claim 5, wherein the controller transfers the selected number of blocks of data having the selected block size from the tail FIFO to the memory based on the tail fill indicator.

Claim 7 (Previously presented): The system of claim 1, wherein the incoming frames are of varying length and where the selected number of blocks are defined to include data from one or more of the frames, and wherein a selected block may contain data from two or more frames.

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Claim 8 (Original): The system of claim 1, wherein the controller includes a control output coupled

to the control input of the multiplexer, wherein the controller is operable to control which of the

multiplexer inputs is coupled to the multiplexer output.

Claim 9 (Original): The system of claim 1, wherein a data path to the memory is wider than a width

characteristic of the tail FIFO.

Claim 10 (Previously presented): A method for implementing a caching system, the method

comprising steps of:

receiving frames containing varying amounts of data at a tail FIFO

selecting a maximum efficiency level for operating a memory interface;

dynamically determining a block size and number of blocks to support the maximum

efficiency level;

transferring the number of blocks of the data having the determined block size from the

tail FIFO to a head FIFO when the head FIFO is within a first fill level, wherein the head FIFO

includes an output to output the data;

transferring the number of blocks of the data having the determined block size, from the

tail FIFO to a memory via the memory interface, when the head FIFO is within a second fill

level;

transferring the number of blocks of data from the memory to the head FIFO when the

head FIFO is within a third fill level.

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Claim 11 (Previously presented): The method of claim 10, wherein the frames are of varying length,

and the method further comprises a step of defining the number of blocks of data having the

determined block size to include data from one or more of the frames, and wherein a selected block

of data may include data from two or more frames.

Claim 12 (Previously presented): A caching system comprising:

    a tail FIFO having

        a tail input to receive incoming frames containing varying amounts of data

        a tail output to output data

    a memory having a memory input and a memory output, the memory operable to

        store data that is output from the tail output

        output data at a memory output

    a multiplexer having first and second multiplexer inputs coupled to the tail output and the

memory output, respectively, the multiplexer having a control input to select one of the

multiplexer inputs to couple to a multiplexer output

    a head FIFO having

        a head input coupled to the multiplexer output to receive data

        a head output to output data, the output data comprising data frames of variable

length

    a controller

        coupled to at least one of the tail FIFO and the head FIFO

coupled to the memory

operable to control transfers of dynamically selected numbers of blocks of data

having dynamically selected block sizes between the memory and the at least one of the tail FIFO

and the head FIFO at a maximum efficiency.

Claim 13 (Previously presented): The caching system of claim 12 wherein

the incoming data and the output data comprise frames of variable length

the memory stores data in blocks of at least one fixed size.

Claim 14 (Previously presented): The caching system of claim 12 wherein the controller is further

operable to control memory transfers from the tail FIFO to the memory in fixed-length blocks,

wherein the selected efficiency is achieved at least in part by maximizing an amount of data taken

from the tail FIFO and put in the blocks.

Claim 15 (Previously presented): The caching system of claim 12 wherein the controller is further

operable to control transfers of data from the memory to the head FIFO in fixed-length blocks,

wherein the selected efficiency is achieved at least in part by maximizing an amount of data destined

for the head FIFO in the blocks.